REQUEST FOR ACTION (RFA) RESPONSE

GLAST LAT Project
Calorimeter Peer Review **17 – 18 March 2003**

Action Item:	CAL – 030
Presentation Section:	Electrical - Miscellaneous
Submitted by:	J. Sonsino

Request:

1. In general block diagrams are too high level. For a CDR presentation need to have more detailed and complete diagrams. Diagrams don't seem to link up by signal names.
2. In GCRC design details diagram (7-32):
   - Itemize commands being handled
   - Show data formats and contents
   - Temperature telemetry – how many? Health telemetry?
3. Need to show timing diagrams and analog waveforms associated with block diagrams. (7-34 is a good example.)
4. Need to provide or reference documents related to the optical/electronics front-end design explaining the physics of light → electrical conversion, equations, etc.
5. Design and revision history may not be necessary for presentation. If at all – may be provided as backup material on web page.
6. Show a typical LVDS circuit details.
7. A/D and DAC basis characteristics – how many bits? How fast, etc?

Reason / Comment:

Response:

See attached updated presentation slides (15 pages) that address the requested topics.

Improvements to 7.0 Electrical

Jim Ampe

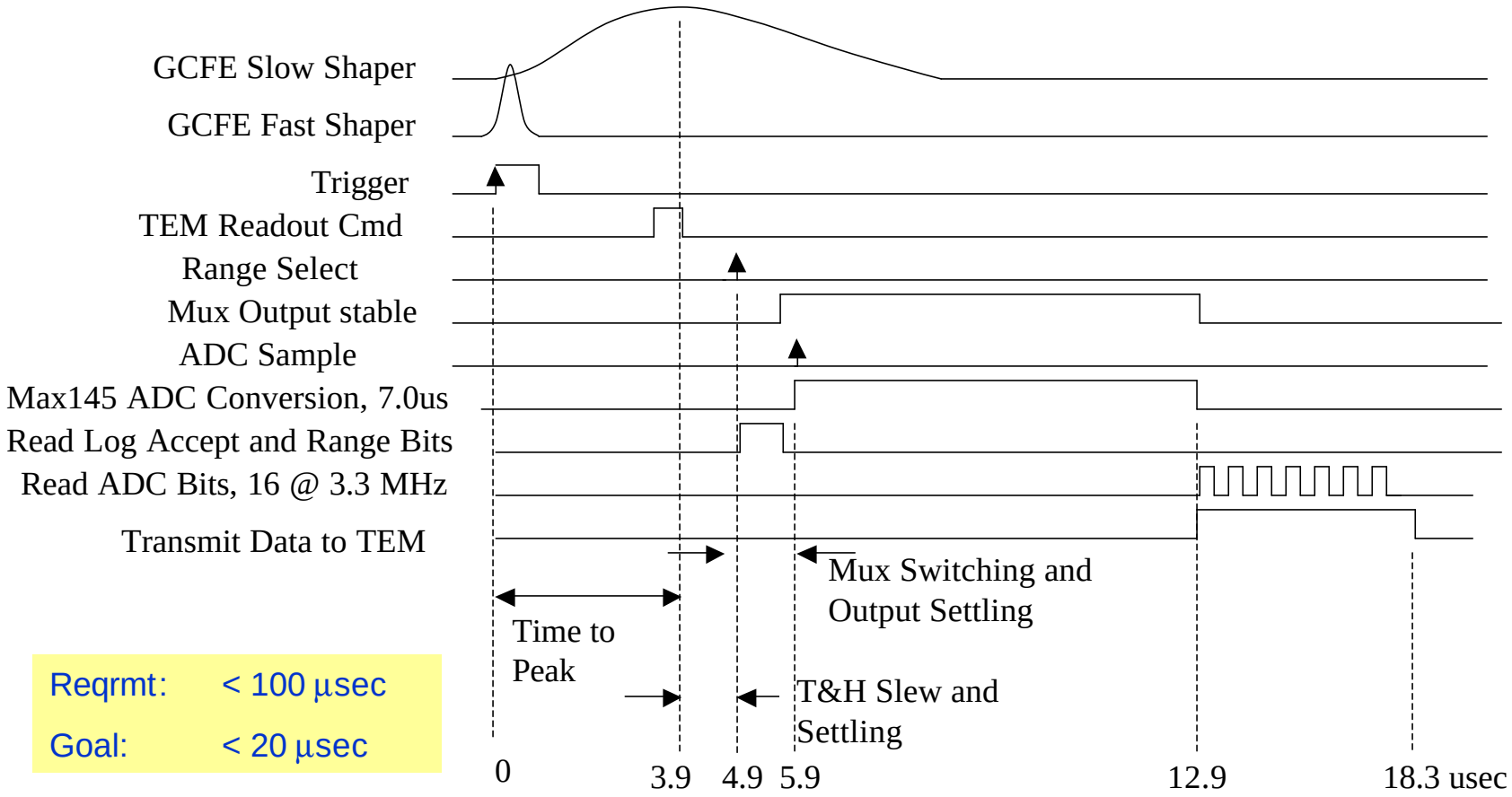
10 April 2003

CDE Principles of Measurement

- **CsI(Tl) crystals scintillate when excited by energy depositions by photons or charged particles.**
  - **Peak of the emission spectrum is ~ 560 nm**
  - **Approx 40,000 photons are created per MeV of energy deposition in the CsI.**
  - **Scintillation light has three time constants which are approximately represented by a single exponential, τ ~ 1000 ns.**
  - **The number of photons collected by the optical sensor (PIN diode) and converted to electrons depends on many things: crystal quality, crystal geometry, surface treatment, optical wrap, and sensor effective area (size x spectral efficiency).**
    - For CAL CDEs, we collect ~8000 electrons (spec is > 5000) per MeV for depositions in the central region of the CDE from the large PIN diode on one end of the CDE and ~ 1500 electrons from the small diode.
    - These electrons are collected on the feedback capacitor of the charge-sensitive preamp the the GCFE ASIC. The ASIC is AC-coupled to the diode so that the diode dark current does not saturate the front end preamp but is just a contribution to the front end noise.
  - **The GCFE slow shaping amplifier has an integration time long enough to collect most of these electrons for pulse amplitude measurements.**
  - **The GCFE fast shaping amplifier has lower sensitivity (ballistic defficit and higher noise) but provides accurate timing signals to the trigger system.**

Readout Timing Diagram

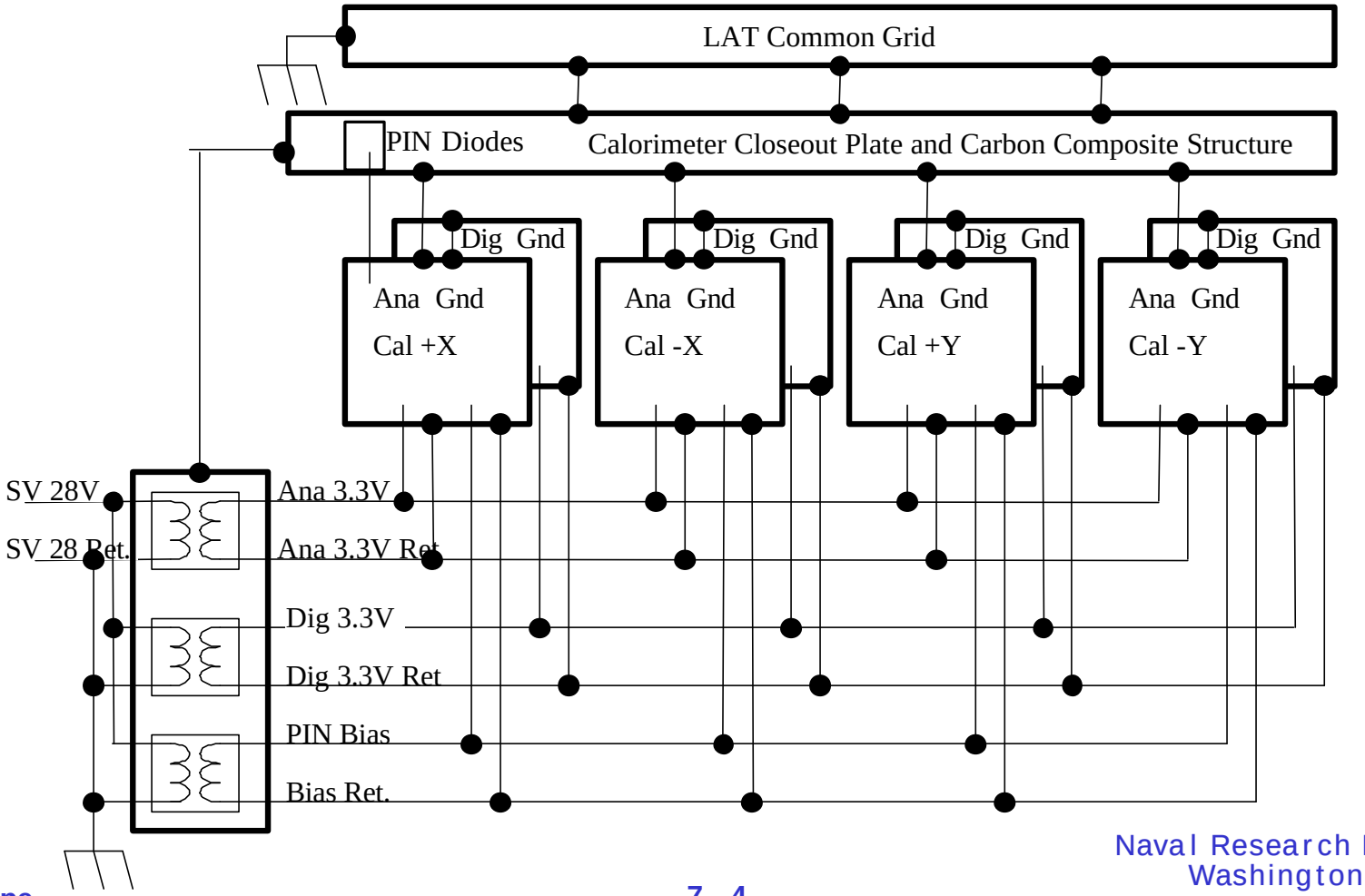
- **Shown is a readout timing diagram of the Calorimeter.**



Reqrmt:	< 100 µsec
Goal:	< 20 µsec

Architecture, Grounding Diagram

- **Calorimeter Circuit boards are grounded to the Cal structure for low noise PIN diode signal.**
  - **Structure comprised of aluminum, titanium, stainless steel, and carbon composite.**
  - **Low resistive path, measured < 0.5 ohm, between any 2 points in structure.**
  - **Diodes are located around periphery of carbon composite structure.**



GCFE Commanding

- **GCFE Commands Consist of Register Reads and Writes.**
  - **Register read command comprised of prefix read bits and command function bits.**
  - **Register write command comprised of prefix write, command function and data bits.**

Command Name	Cmd Prefix, Read Bits	Cmd Prefix, Write Bits	Cmd Prefix, Dataless Cmd	Command Function Bits	Command Data Bits	Command Description
Register, Configuration 0	10	01		000	13 Bits	Preamp Gains, Readout Order Settings
Register, Configuration 1	10	01		001	7 Bits	Trigger Enables
Register, Fast Low Energy DAC	10	01		010	7 Bits	LE Trigger Threshold
Register, Fast High Energy DAC	10	01		011	7 bits	HE Trigger Threshold
Register, Log Accept DAC	10	01		100	7 Bits	Log Accept Threshold for Sparseification
Register, Upper Level Discriminator DAC	10	01		101	7 Bits	Discriminator for Automatic Range Selection
Register, Reference DAC	10	01		110	7 Bits	Test Output DAC

GCFE Configuration Settings

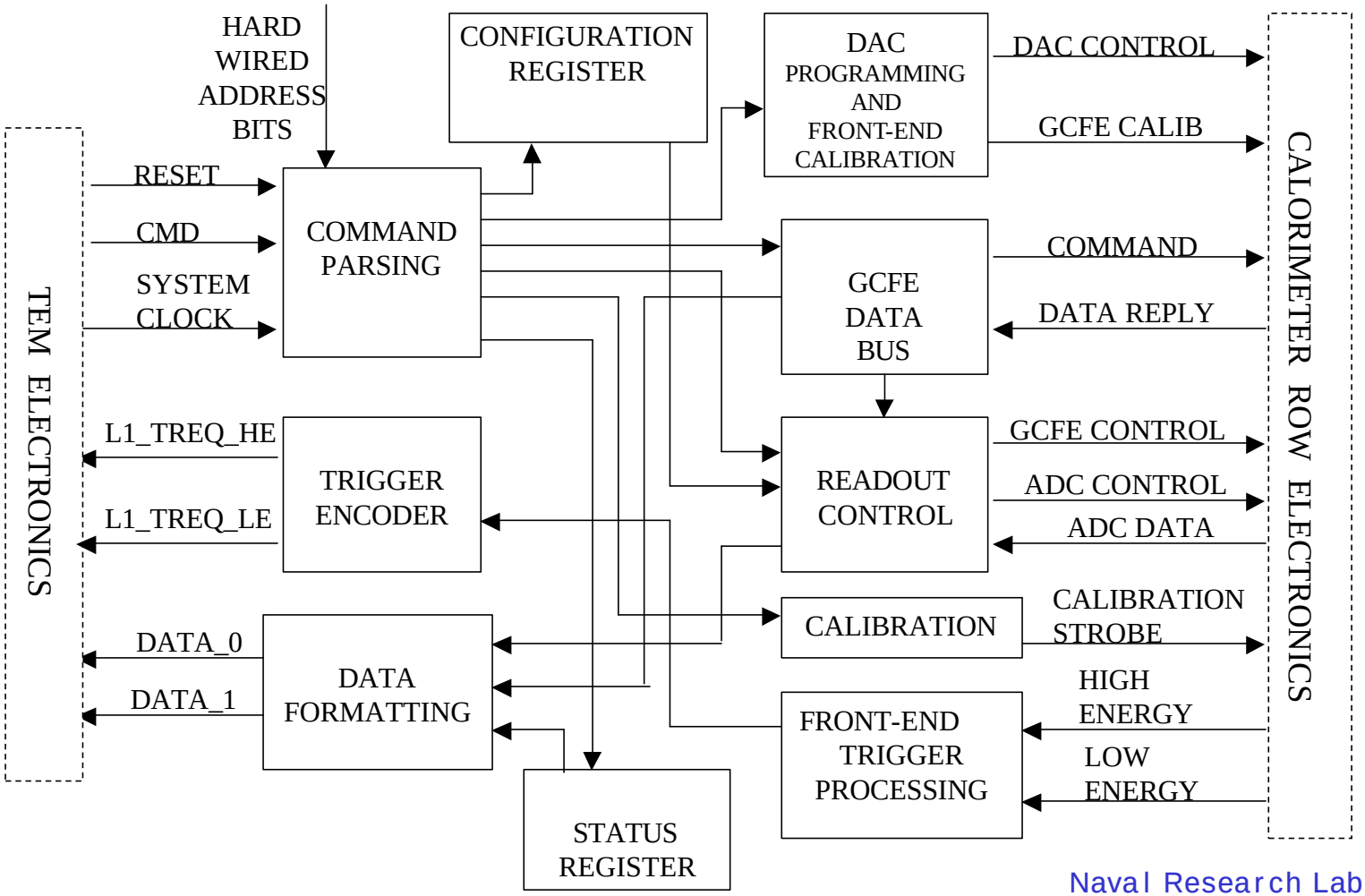
GCFE has Two Configuration Registers

Configuration Register 0	Number of Bits	Description
LE Preamp Gain Selection	3	Low Energy Preamp Gain, Selectable Factor 3.9 from Lowest to Highest Gain.
HE Preamp Gain Selection	4	High Energy Preamp Gain. High Gain for Ground Muons and Selectable Gain Factor 3.9 for Flight.
Autoranging Enable Bits	2	Separately Enable Low Energy and High Energy Autoranging Circuit.
Autoranging Order Bits	4	Enables any of the 4 Ranges to be Output First.

Configuration Register 1	Number of Bits	Description
Preamp Auto Reset Enable	1	Enables Preamp Auto-Reset for Large Input Signals.
LE and HE Trigger Enables	2	Separately Enable Low and High Energy Trigger Outputs.
Calibration Charge Injection Select Bits	3	Select 1 of 2 charge Injection Capacitor Configurations and Separately Enable Low and High Energy Charge Injection.

GCRC Functional Block Diagram

GCRC Digital ASIC Functional Block Diagram



GCRC Design Details

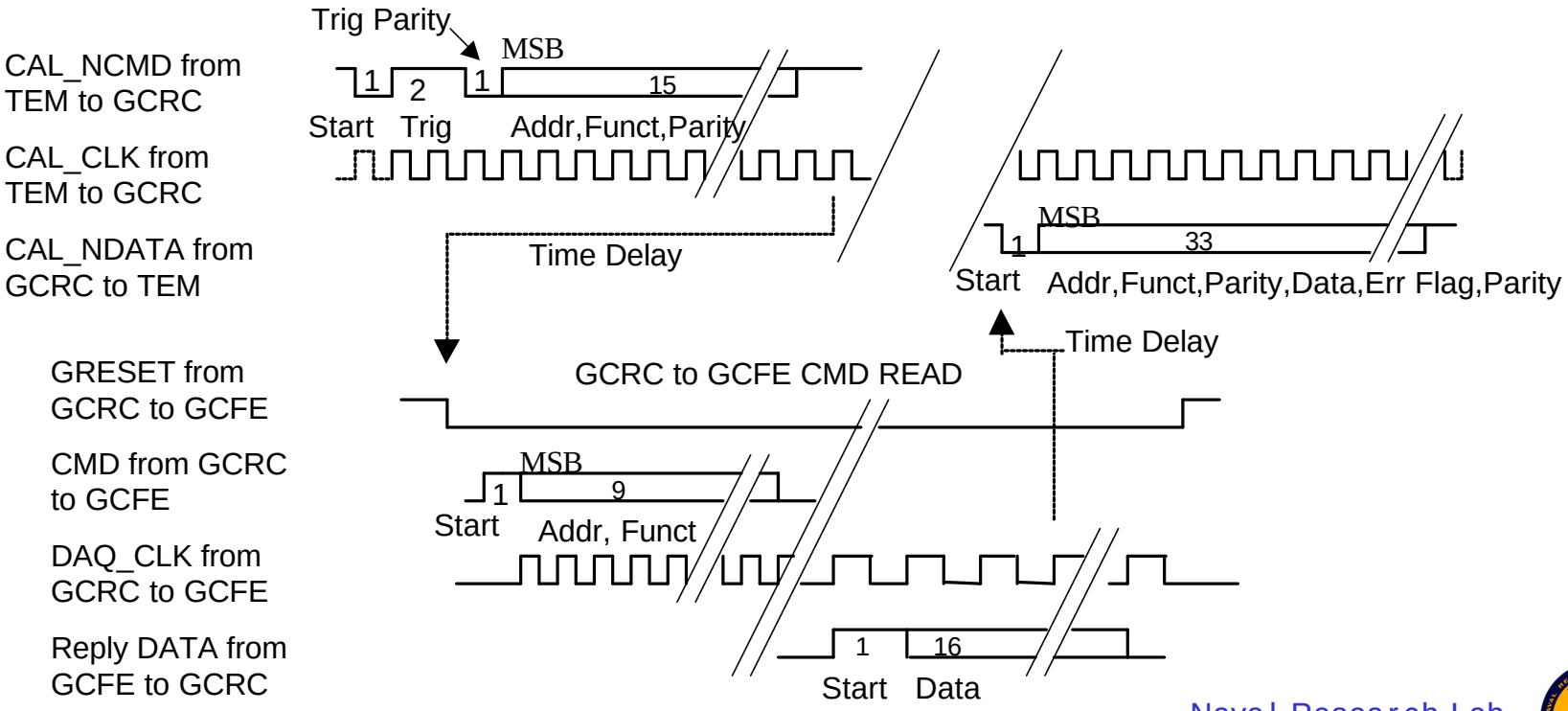
- **GCRC Digital ASIC, main Features**
  - 1 GCRC per Cal row interfaces 12 GCFEs, 12 ADCs, and 1 DAC to the TEM
  - LVDS communication used for all communication except to ADC and DAC chips
  - Each GCRC has a hard wired address to receive bussed commands from the TEM
  - Package 80 Pin Plastic Quad Flat Pack 14mm square body

GCRC Commanding

Command	Cmd Prefix, Read Bits	Cmd Prefix, Write Bits	Cmd Prefix, Dataless Cmd	Command Function Bits	Command Data Bits	Command Description
GCRC Reset			00	001		Resets GCRC
Calibration Strobe			00	011		Initiates 6.2 usec Calibration Pulse
Register, Range Decision Delay	10	01		011	6 Bits	Delay from Hold to Range Decision
Register, ADC Sample Delay	10	01		100	6 bits	Delay from Range Decision to ADC Sample
Register, ADC Conversion Time	10	01		101	8 Bits	Time for all ADCs to Convert.
On Board Calibration DAC Setting	10	01		110	16 Bits	On board DAC for Calibration Charge Injection
Register, GCRC Configuration	10	01		111	3 Bits	Sets GCRC Communication Pairity
Register, GCRC Status	10			000	5 Bits	GCRC Error Bits
Register, Last Error Command	10			001	16 Bits	Readback of Last TEM Command in Error

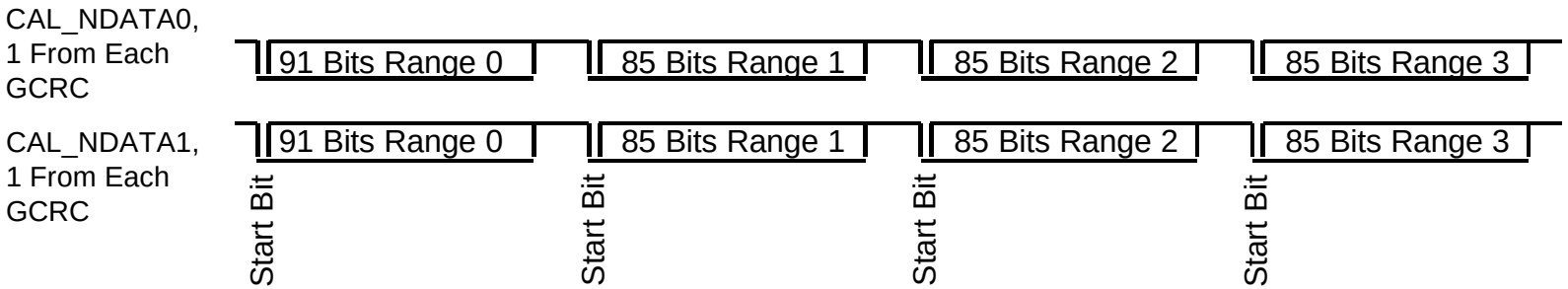
GCRC to GCFE Communication

- **Communication Example, Read GCFE Register**
  - **GCRC Decodes Read GCFE Command from TEM, Passes Command to GCFE**
    - **GCRC checks command for proper parity, then strips parity and GCRC address bits.**
  - **GCRC Waits for GCFE Reply Data, then Formats Transmission back to TEM**
    - **GCRC Reads GCFE reply at half the system rate, transmits to TEM at full clock rate.**



Event Readout Data to TEM

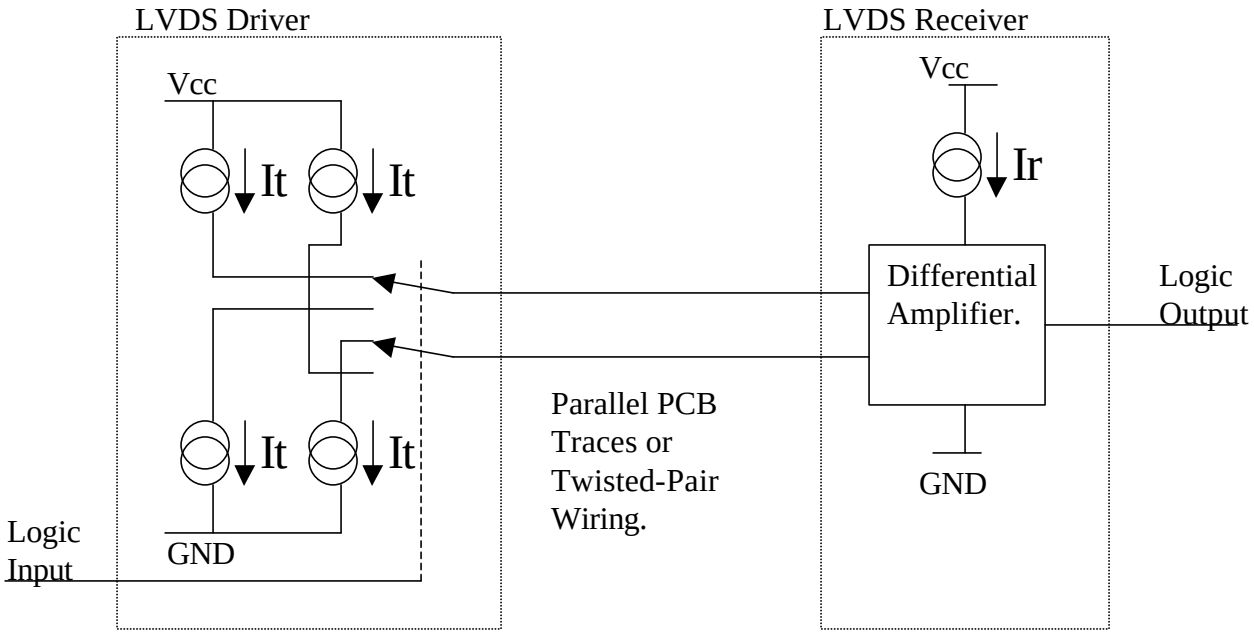
- **Calorimeter Transmits Fixed Event Data Packet Size to TEM.**
  - **Event Data per Log-End per Range: 12 ADC bits and 2 Range Identification Bits.**
  - **Per Event, Additional 1 Log-Accept bit per Log-end for TEM Data Sparsification.**
  - **Nominal Flight Event Readout Mode is Single Range Readout.**
    - **TEM Receives: 2*91 Bits per GCRC, 728 Bits per AFEE, 2912 bits per Cal Unit.**
    - **Average expected sparisification per event is 20 Crystals**
      - **For 20 Crystals, TEM reduces Event Data Size from 2912 Bits down to 560 Bits.**
  - **Flight 4 Range Readout Mode for Heavy Ion Calibration**
    - **TEM Receives: 2*346 bits per GCRC, 1384 bits per AFEE, 5536 bits per Cal Unit.**



GCRC Four Range Readout Bit Count to TEM. First Range Readout sends Log-Accept Bits, thus 6 Additional Bits per Half AFEE Row.

LVDS Driver / Receiver Circuit

- **Non-Standard LVDS Driver Current used for communications.**
  - **Standard Commercial LVDS Drivers use 3.5mA Signaling Current.**
  - **GCRC and GCFE LVDS Driver Circuits use Lower Signaling Current.**
    - **GCFE It 0.4 mA nominal Drive, Added resistor on EM AFEE boosts It to 1.1mA**
    - **GCRC It 0.8 mA nominal Drive, Added resistor on EM AFEE boosts It to 1.4mA**
  - **Receiver Design is Standard Differential Amplifier to Single-ended Logic.**
    - **GCFEv7 and GCRCv4 have Receiver Bias Ir of 10uA**
    - **GCFEv9 and GCRCv5 have Receiver Bias Ir of 50uA**



AFEE ADC and DAC

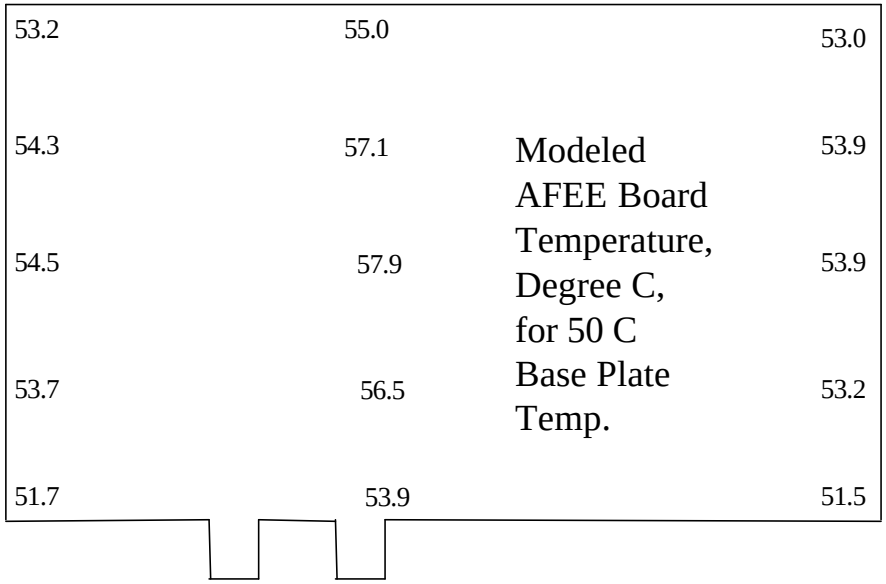
- **ADC is Maxim Max145**
  - 12 Bit Switched Capacitor ADC with Internal Conversion Clock.
  - 3.3V Operating Supply
  - 8 lead uMax SOIC package.
  - 2.5 usec Acquisition Time, 7.0 Conversion Time, 3.2 usec Min Readout Time.
  - 4.5 mW Power Consumption During Conversion.
  - Measured Low Differential Non-Linearity.
  - Measured Ion Beam LET Latchup Threshold > 80 MeV /(mg/cm^2)
  - Measured SEU Upset Threshold > 80 MeV /(mg/cm^2)
- **DAC is Maxim Max5121**
  - 12 Bit Voltage Output DAC with internal Reference.
  - 3.3V Supply
  - 16 Lead SOIC package.
  - Measured Laser Radiation LET Latchup Threshold > 900 MeV /(mg/cm^2)
  - Measured SEU Upset Threshold > 900 MeV /(mg/cm^2)

AFEE Thermal Analysis

- **AFEE Thermal Analysis Summary.** From LAT-TD-01114-01 Dated 4/03
  Author Peck Sohn, Swales Aerospace
- **Maximum silicon die temperatures for 50 C Qual Base Plate temperature**

Device	GCRC	GCFE	ADC	DAC	Ref.
Modeled Die Junction Temp. Deg. C	61.3	58.2	58.5	58.4	59.7
Maximum Derated Die Temperature, Deg. C	93	93	93	93	93

- **Analysis result, Calorimeter AFEE electronics do not have any thermal problems**



Assumptions

	Modeled Heat Dissipation	Theta Junction to Board (C/W)
GCRC	65 mW	50
GCFE	11.5 mW	114
ADC	2 mW	183
DAC	4 mW	86
Ref.	7 mW	232
Total Power per AFEE	952 mW	
AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers.		

CAL State of Health Monitoring

- **CAL housekeeping and state of health monitoring are functions of the Tower Electronics Module (TEM) that supports a single CAL module and a single TRK module.**
  - **The TEM captures voltage and current monitors for the CAL power supplies**
  - **CAL provides 8 thermistors (2 per AFEE card) for processing by the TEM.**
  - **The TEM provides 2 rate counters for diagnostic trigger rate monitoring. Multiplex controls select the signals to be monitored by the 2 counters. Timing sequence and readout rate are controlled by T&DF flight software.**
  - **The CAL command state (operating configuration) is captured by the T&DF software via command register readback. Every time a command configuration change is made, the entire command state is verified by readback. This is flight software control option.**